CLAIMS

1. A microprocessor with an architecture incorporating a number of execution units, whereby:

   a number of registers store results from particular execution units;

   execution unit operands may receive data from a number of these registers; and

   certain execution units are able to copy data from their operands to results.

2. The microprocessor according to claim 1 whereby one or more of the execution units may be register files.

3. The microprocessor according to claim 1 whereby the set of registers associated with a particular execution unit to be written may be specified for each operation.

4. The microprocessor according to claim 3 whereby the specification of registers to write is represented in the instruction format.

5. The microprocessor according to claim 4 whereby the specification of registers to write is delayed in a pipeline so as to be available on the same clock cycle as the results.

6. The microprocessor according to claim 1 whereby the connectivity between execution units is known to the code generation software tools.

7. The microprocessor according to claim 1 whereby the available execution units are specified in a library file.

8. The microprocessor according to claim 7 whereby the connectivity of execution units to other units in the system is configurable.

9. The microprocessor according to claim 8 whereby the number of output registers associated with an execution unit is configurable.

10. The microprocessor according to claim 1 whereby the update of the output registers is dependent on global condition state for certain execution units.

11. The microprocessor according to claim 10 whereby the state used to control the output register update is selectable as part of the instruction set.

12. The microprocessor according to claim 1 whereby certain identity operations may be issued to an exection unit in order to perform a copy.

13. The microprocessor according to claim 1 whereby the operation of certain bits with an execution word control certain execution units on a cycle by cycle basis.

14. The microprocessor according to claim 13 whereby the number of bits required to control each execution unit varies depending upon the extent of its connectivity.

15. The microprocessor according to claim 13 whereby certain bits within the execution word for each execution unit select different types of operation to be performed.

16. The microprocessor according to claim 1 whereby each output register may be connected to one or more execution unit operands.

17. The microprocessor according to claim 1 whereby the source register for a particular execution unit operand may be specified by the instruction set.

18. The microprocessor according to claim 1 whereby the processor executes a sequence of contiguous execution words.

19. The microprocessor according to claim 18 whereby, when the end the execution word sequence is reached, execution may branch to one of a number of different execution word addresses.

20. The microprocessor according to claim 19 whereby the same execution word sequence may be repeated to resolve a data hazard.

21. The microprocessor according to claim 20 whereby there is a branch control unit for determining the destination of such branches.

22. The microprocessor according to claim 21 whereby the branch control unit may accept branches out of their sequential order.

23. The microprocessor according to claim 22 whereby the branch control unit may disable the operation of certain subsequent operations depending on the sequential position of an accepted branch.

24. A method of operation used in a microprocessor with an architecture incorporating a number of execution units, whereby:

a number of registers store results from particular execution units;

execution unit operands may receive data from a number of these registers; and

certain execution units are able to copy data from their operands to results.

25. The method of claim 24 as used in a microprocessor as defined in any preceding claim 2 – 23.